Karlsruhe Institute of Technology

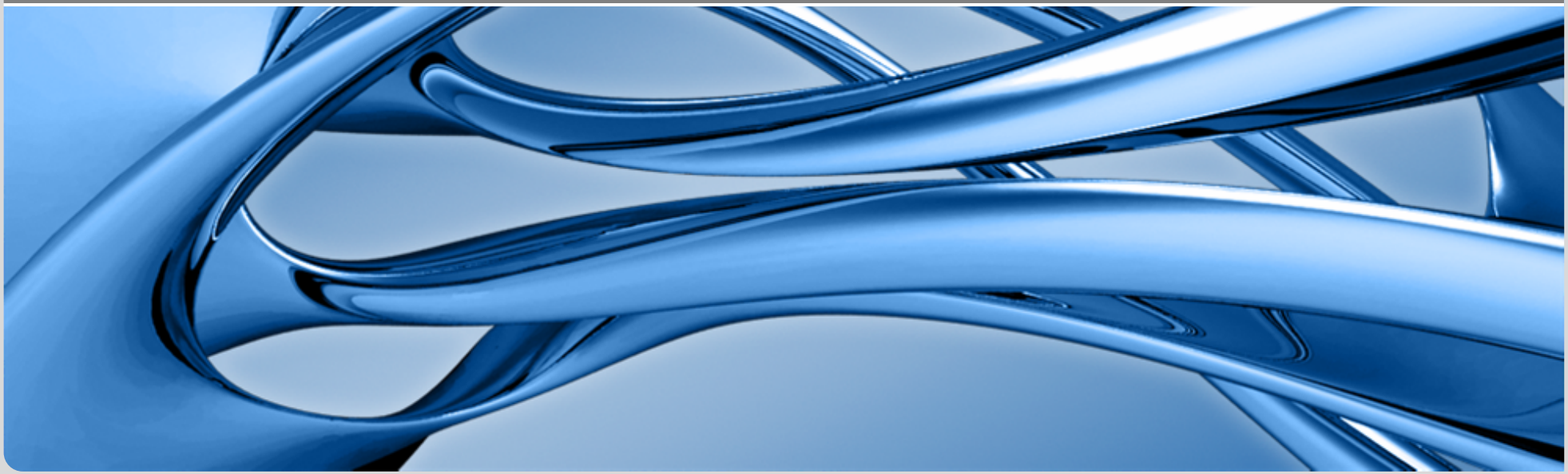
Barcelona Supercomputing Center
Centro Nacional de Supercomputación

Enhancing an HTM System with Monitoring, Visualization and Analysis Capabilities

Philipp Kirchhofer[1], Martin Schindewolf[1], Nehir Sonmez[2], Oriol Arcas[2], Osman S. Unsal[2], Adrián Cristal[2], Wolfgang Karl[1]

[1] **Karlsruhe Institute of Technology (KIT)** [2] **Barcelona Supercomputing Center (BSC)**

Chair for Computer Architecture and Parallel Processing, Institute of Computer Engineering, Karlsruhe Institute of Technology



Motivation

Transactional Memory simplifies parallel programming

But how to achieve good performance and scalability?

Need for a monitoring infrastructure to

- identify runtime characteristics of an application running on an HTM system
- detect application bottlenecks
- get insight into interaction between application and HTM system

Project Goals

Develop a monitoring infrastructure for the TMbox HTM system using event logs:

- Generate events at run time and save for later processing
- Recreate HTM state offline
- Visualize and analyse saved information

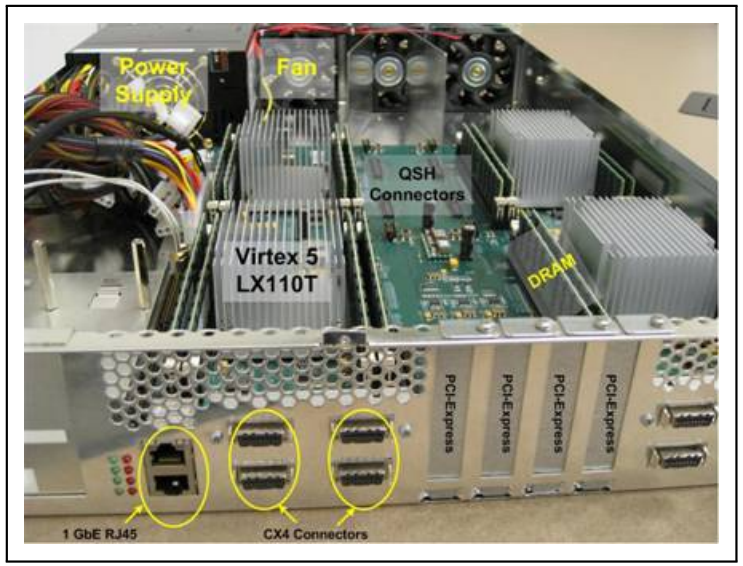
Additional goals:

No probe effect, small hardware overhead, high extensibility, ease of use

Design

The TMbox system

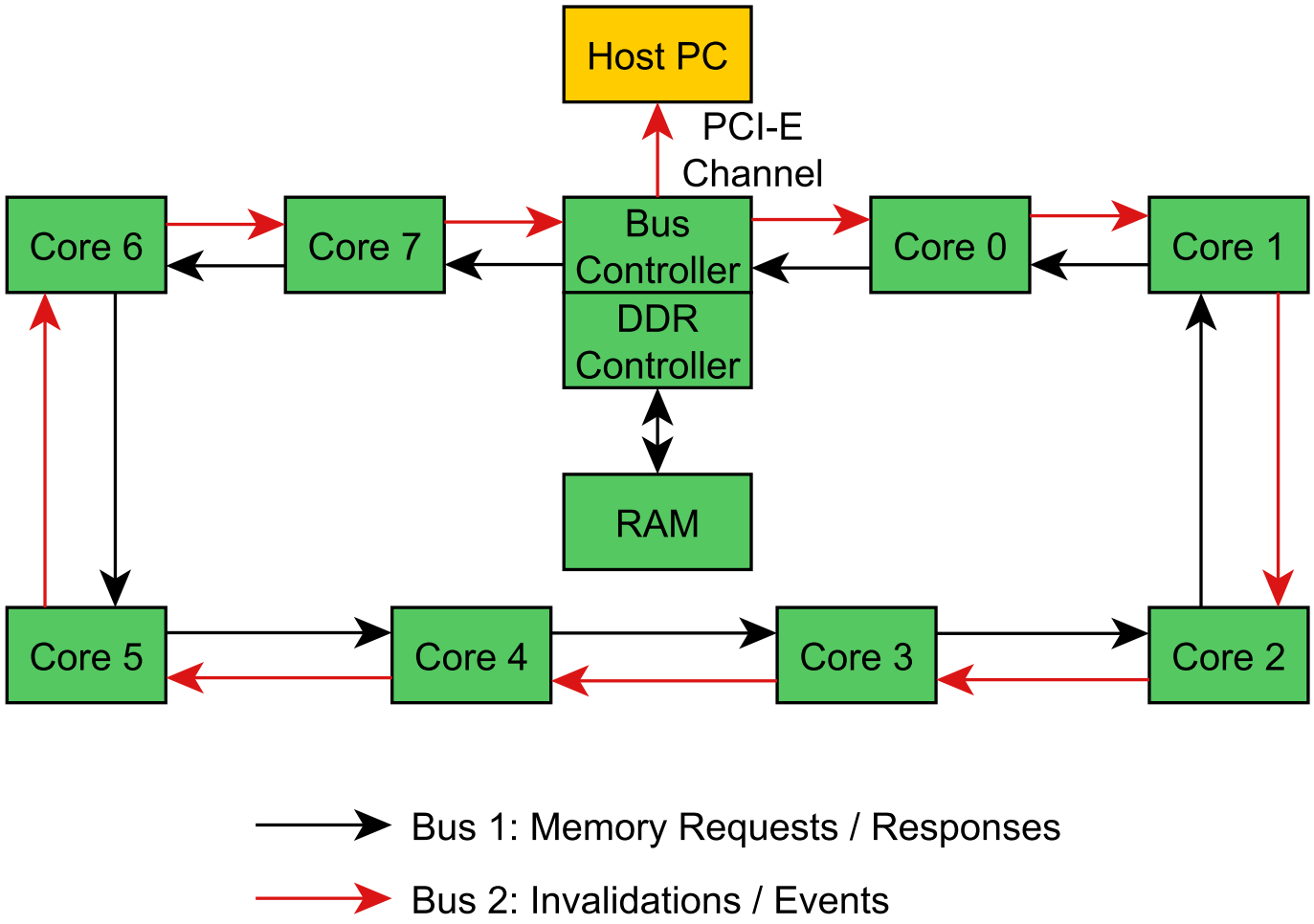
- Developed at Barcelona Supercomputing Center
- MIPS compatible multi-core system (FPGA based, 16 cores on 1 FPGA)



- Supports
  - STM (TinySTM)
  - HTM (BeeTM)
  - HybridTM (Modified TinySTM)

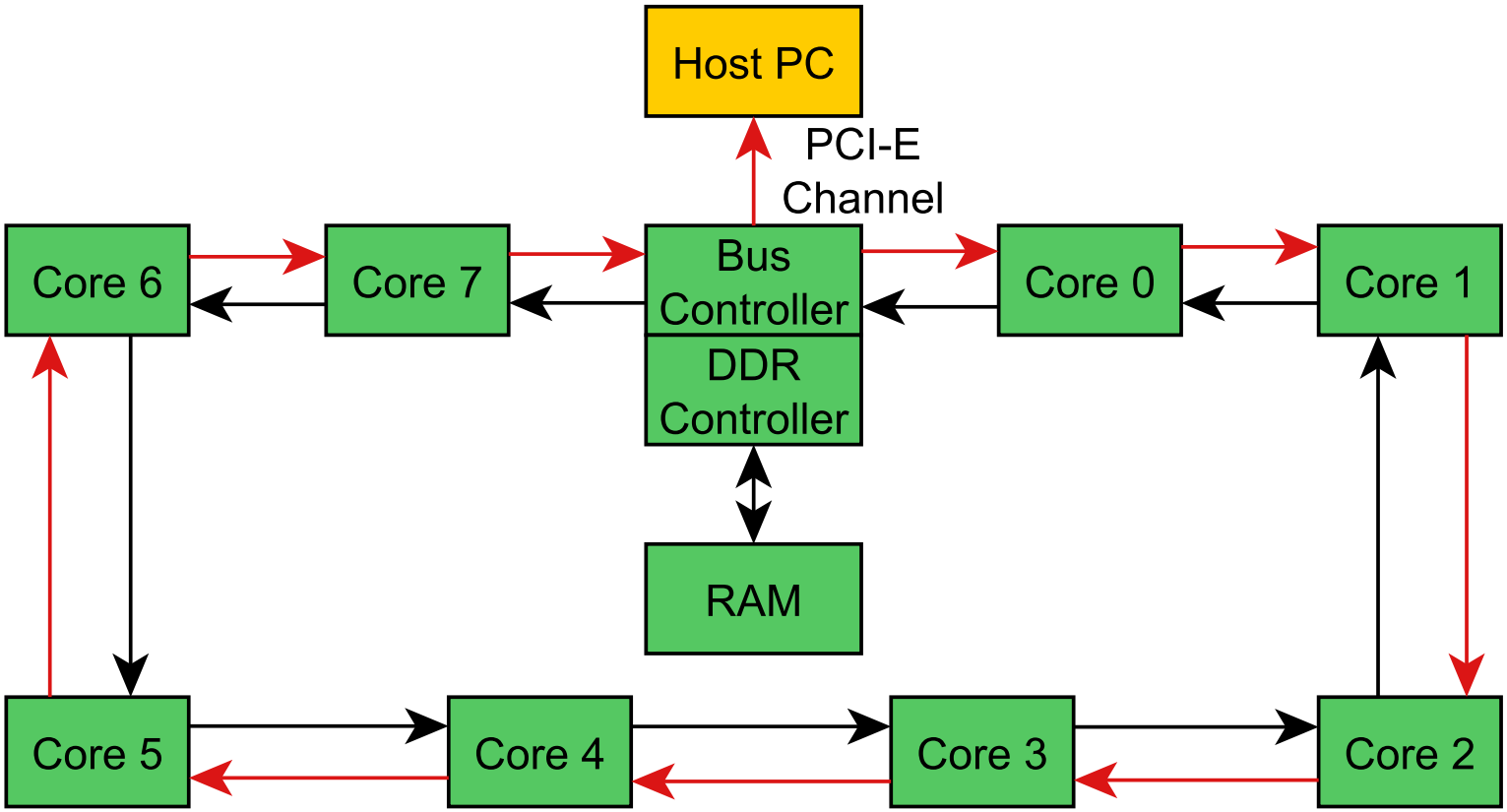
Design

The TMbox system - Block Diagram



Design

Event Generation, Log Unit, Bus Controller



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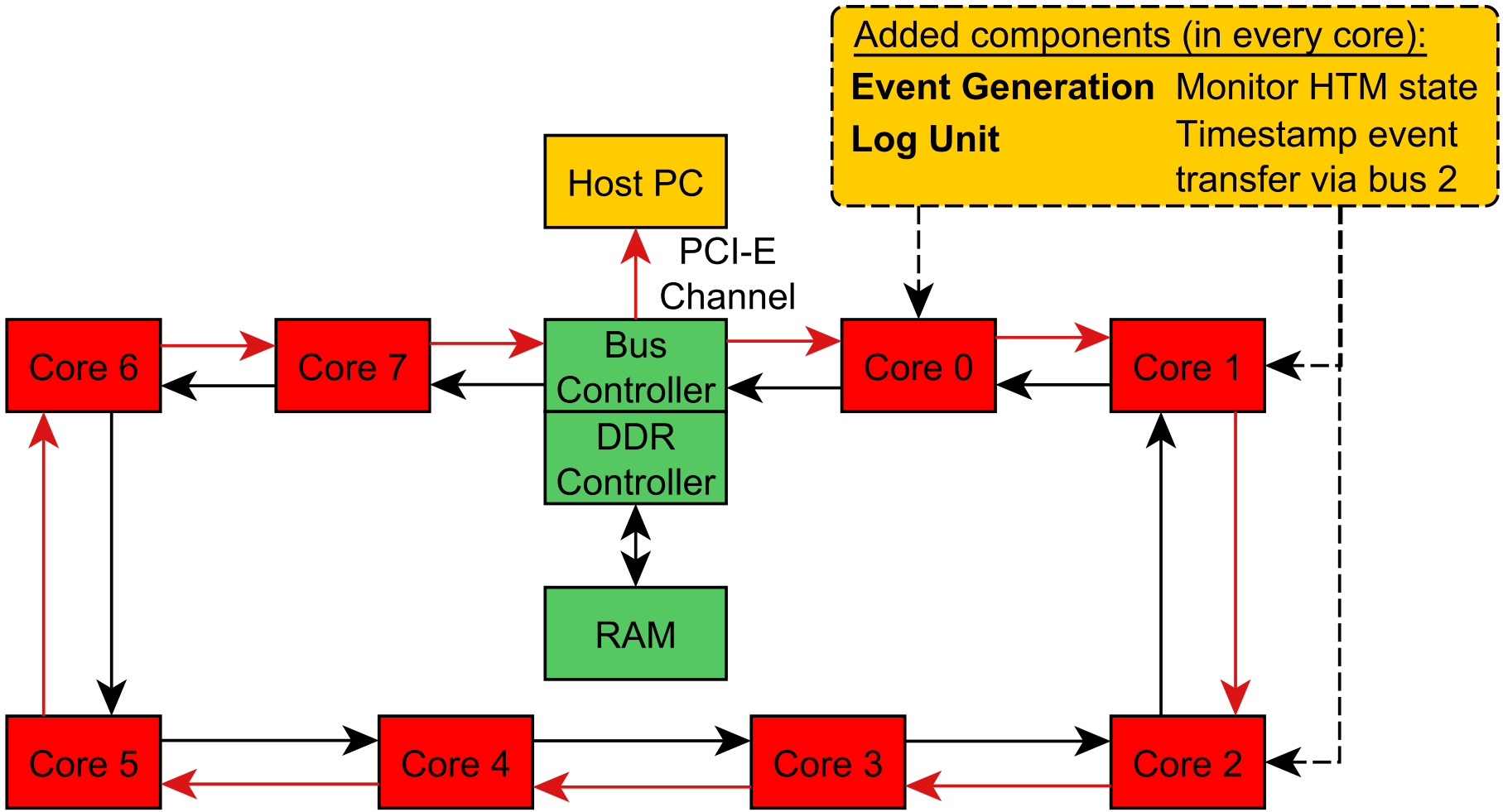
Event Generation, Log Unit, Bus Controller



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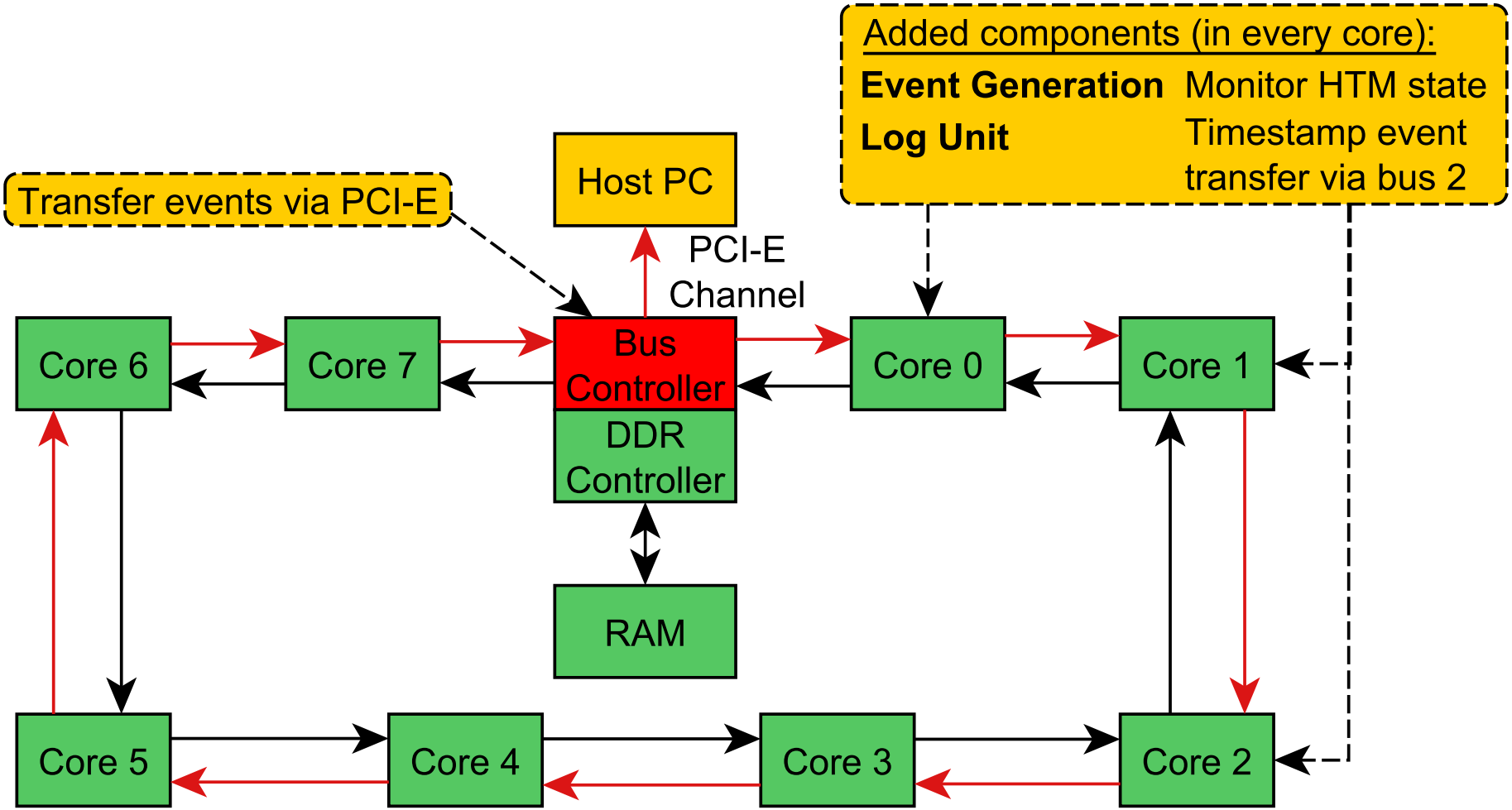
Event Generation, Log Unit, Bus Controller



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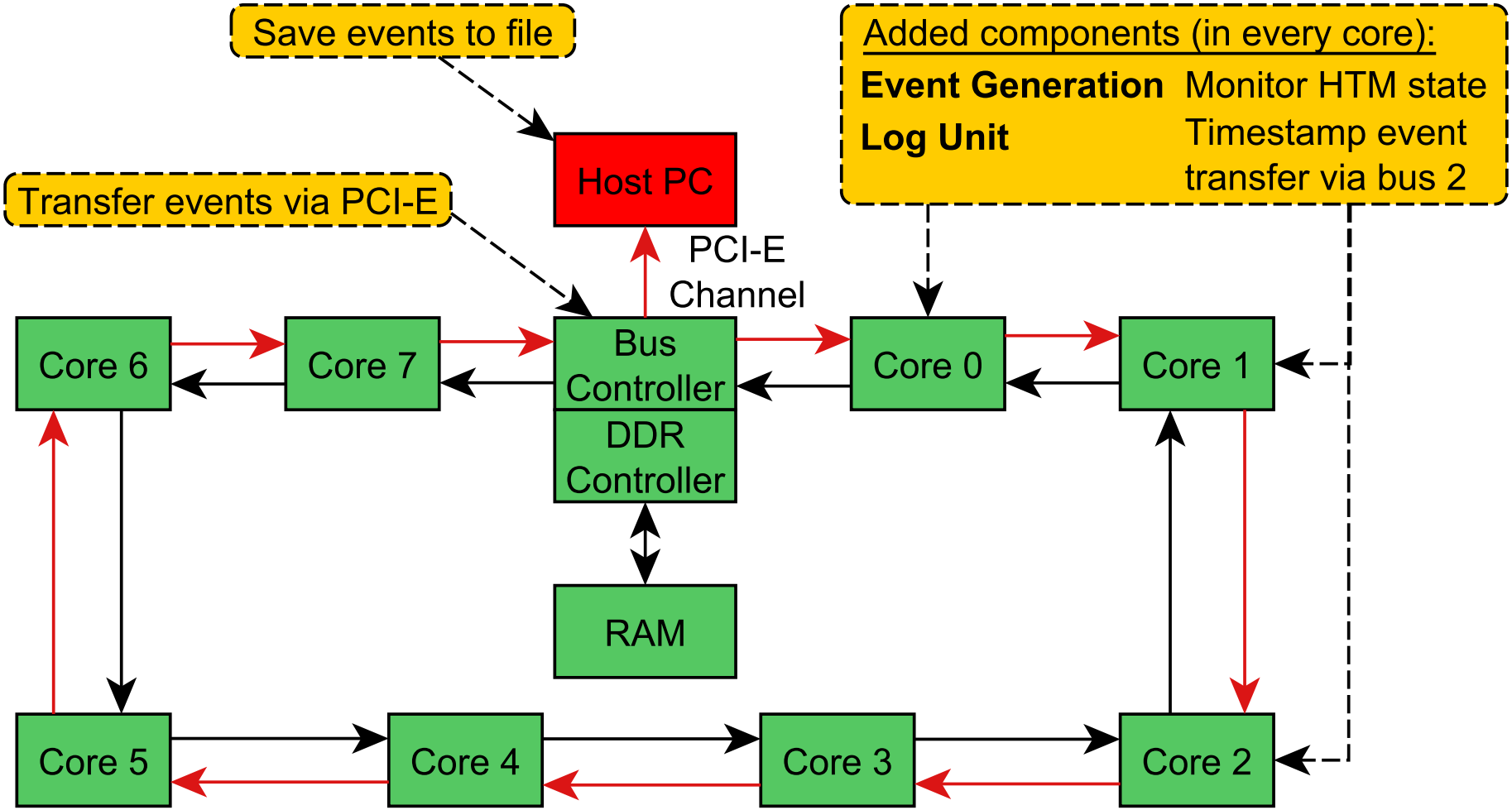
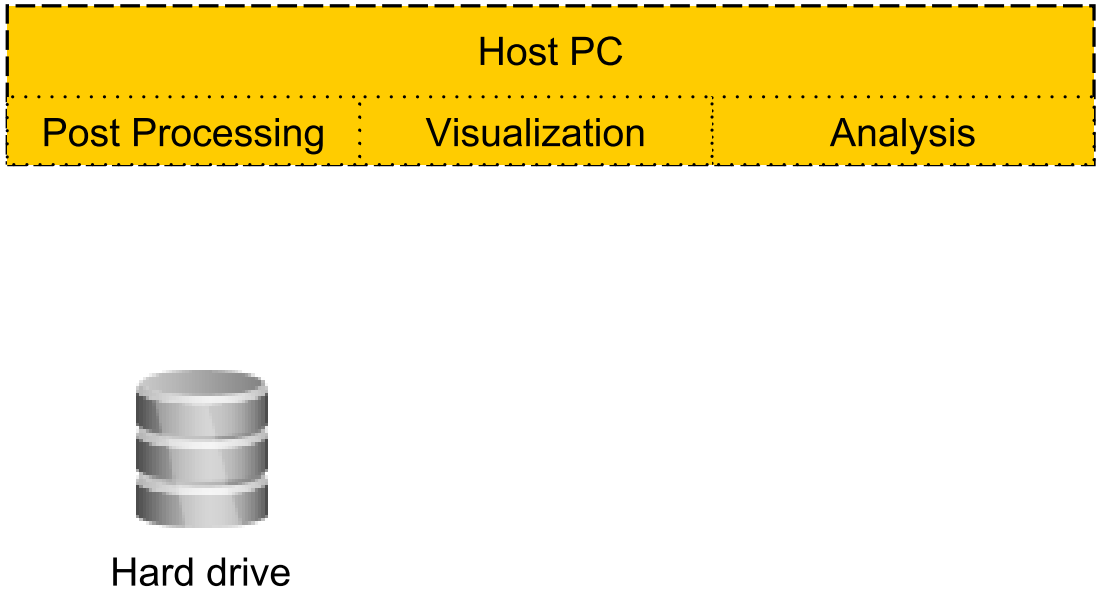
Event Generation, Log Unit, Bus Controller



Design

Post Processing, Visualization, Analysis



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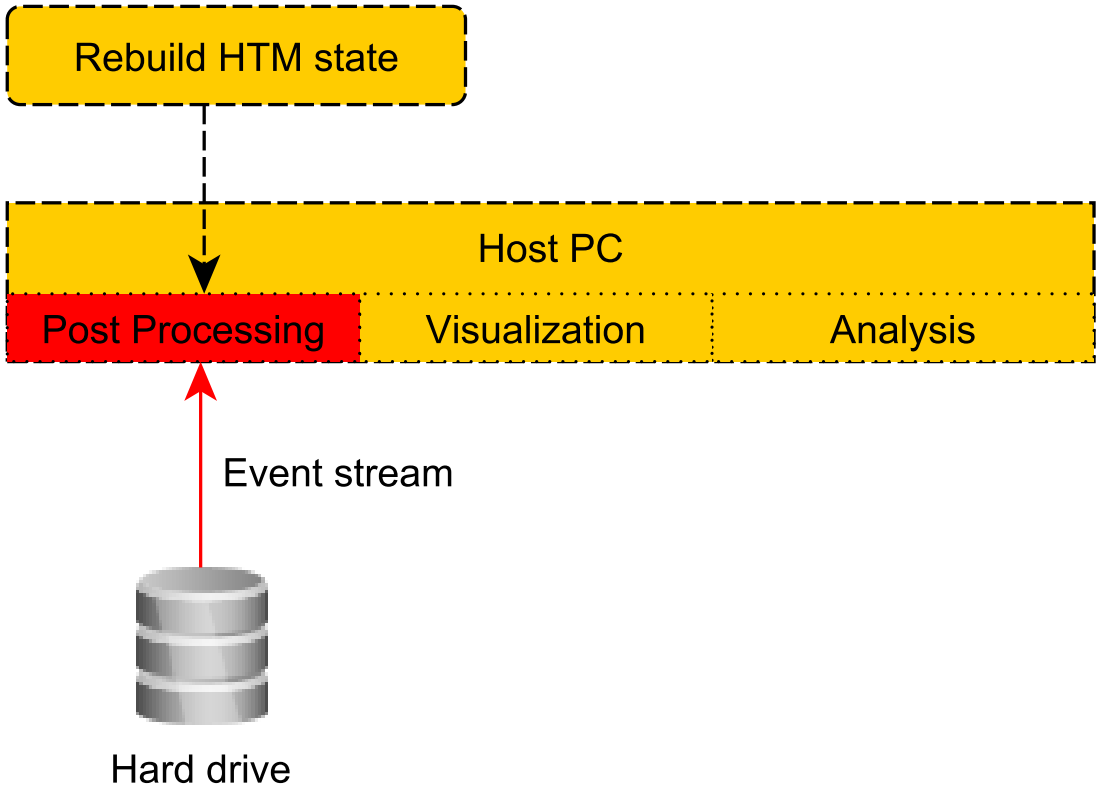
Post Processing, Visualization, Analysis



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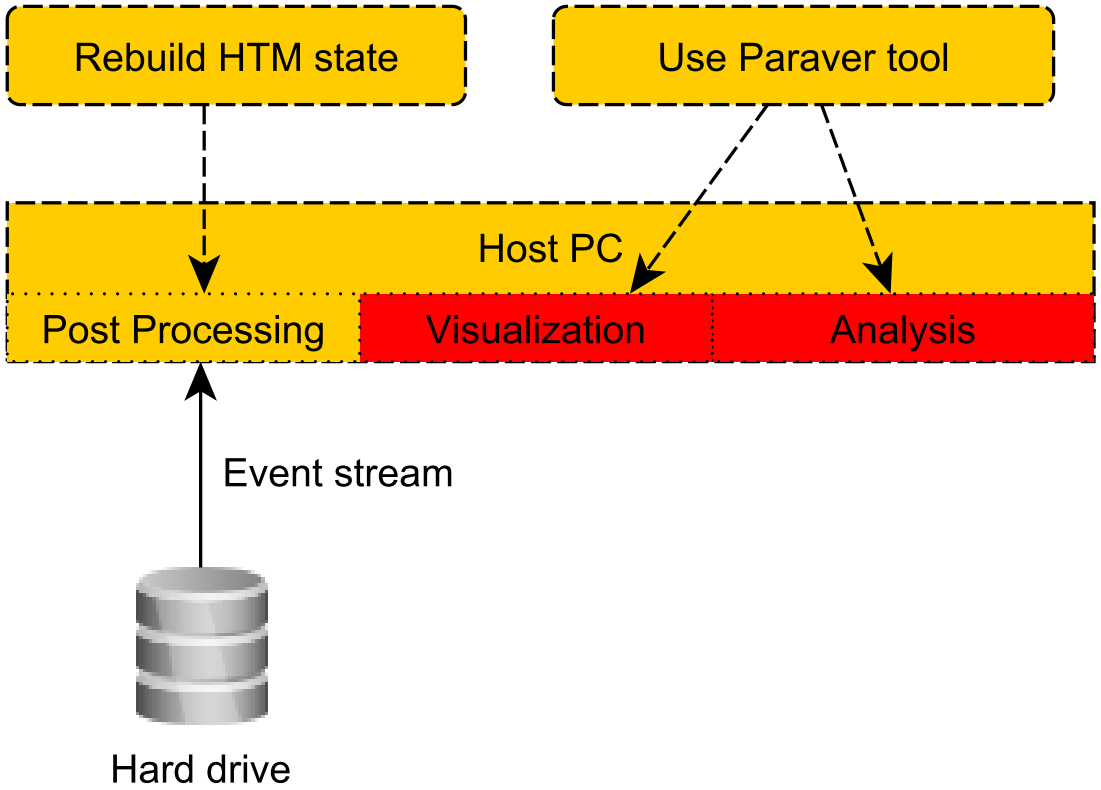
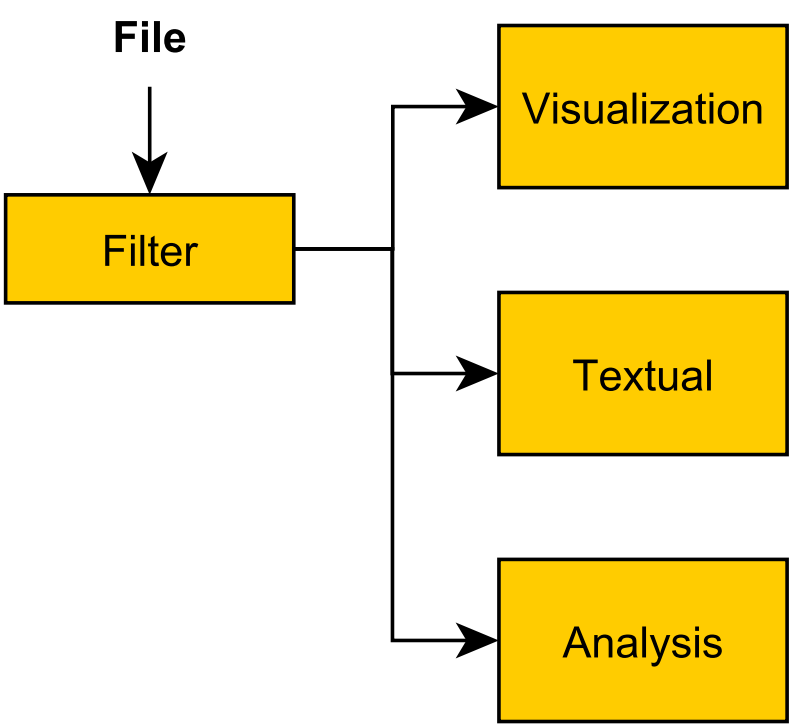
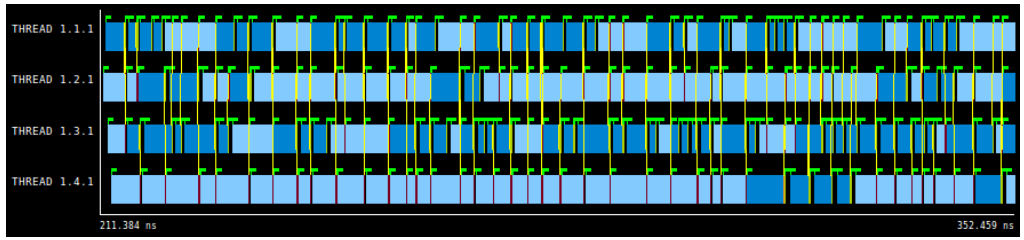
Post Processing, Visualization, Analysis



Results

Paraver workflow





Datei Bearbeiten Ansicht Suchen Werkzeuge Dokumente Hilfe

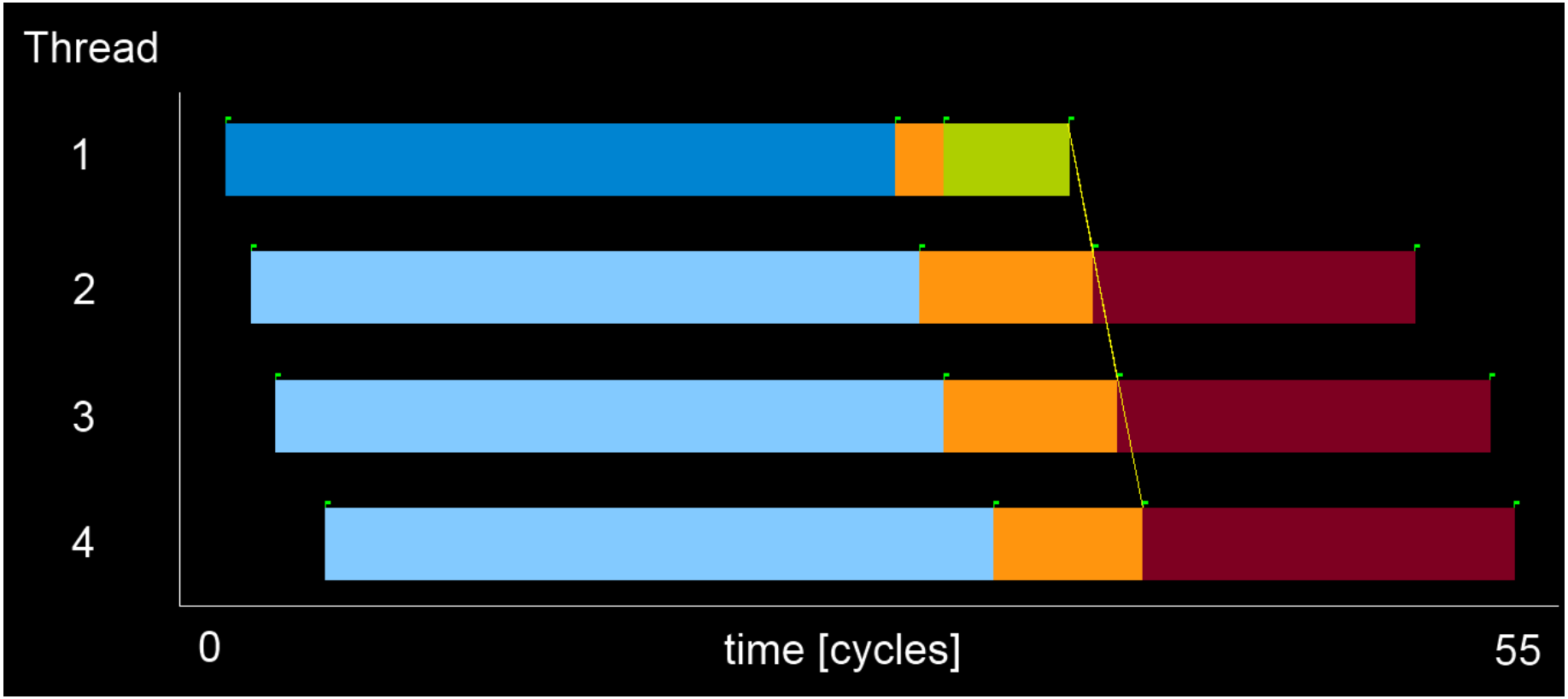
paraver-text.txt

	Compute	Compute_Wasted	Try_Lock	Commit_Locked	Abort	
THREAD 1.1.1	69362.000000	50254.000000	87.000000	877.000000	826.000000	
THREAD 1.2.1	28211.000000	96925.000000	36.000000	372.000000	1628.000000	
THREAD 1.3.1	80721.000000	32511.000000	248.000000	1593.000000	505.000000	
THREAD 1.4.1	17179.000000	107954.000000	43.000000	386.000000	1569.000000	

	Compute	Compute_Wasted	Try_Lock	Commit_Locked	Abort
THREAD 1.1.1	69.362 ns	50.254 ns	87 ns	877 ns	826 ns
THREAD 1.2.1	28.211 ns	96.925 ns	36 ns	372 ns	1.628 ns
THREAD 1.3.1	80.721 ns	32.511 ns	248 ns	1.593 ns	505 ns
THREAD 1.4.1	17.179 ns	107.954 ns	43 ns	386 ns	1.569 ns

Results

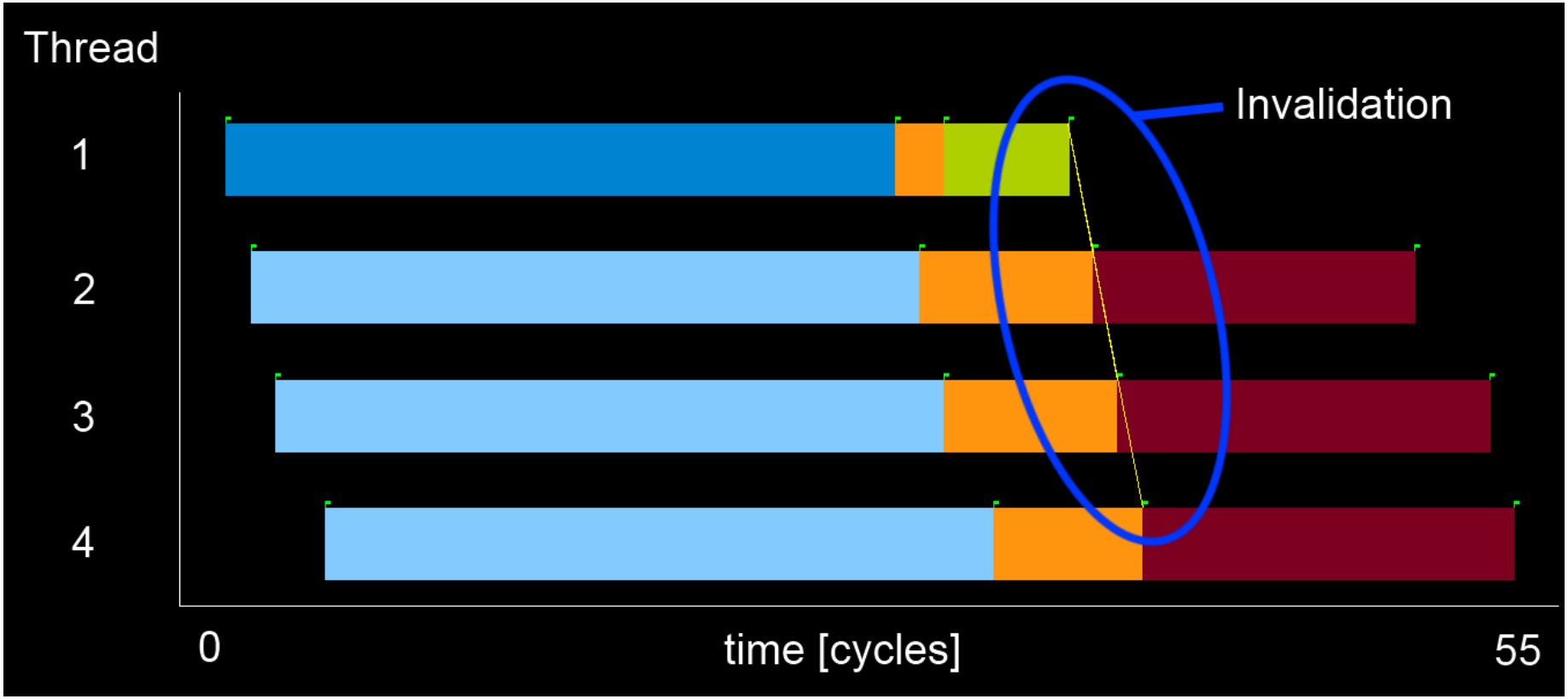
Example: 4 conflicting threads



Idle
Compute
Compute Wasted
Try Lock
Commit
Abort

Results

Example: 4 conflicting threads



Idle
Compute
Compute Wasted
Try Lock
Commit
Abort

Summary

- ✓ Application / HTM runtime behavior is trackable with no probe effects
- ✓ Visualization capabilities lead to in-depth understanding of application / HTM runtime behavior
- Metrics provided via offline analysis, e.g.
  - Time spent in Committed & Aborted Transactions
  - Contention / Commit & Abort Rate
  - Contention between specific threads
  - HTM System Overhead

Summary at a glance

The TMbox system now supports:

- ✓ Identification of detailed runtime characteristics of an application
- ✓ Easy detection of application bottlenecks
- ✓ Getting hints to optimize application concerning both performance and scalability

Ongoing work

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Combine monitoring with STM runtime environment:
Allows analysis of HybridTM systems

See further work in full paper "A low-overhead profiling and visualization framework for Hybrid Transactional Memory" (to appear in FCCM 2012)

Acknowledgment

This work was supported by a Short Term Scientific Mission (STSM) grant from the European Cooperation in Science and Technology (COST) Action IC1001 (EuroTM) during June and July 2011.

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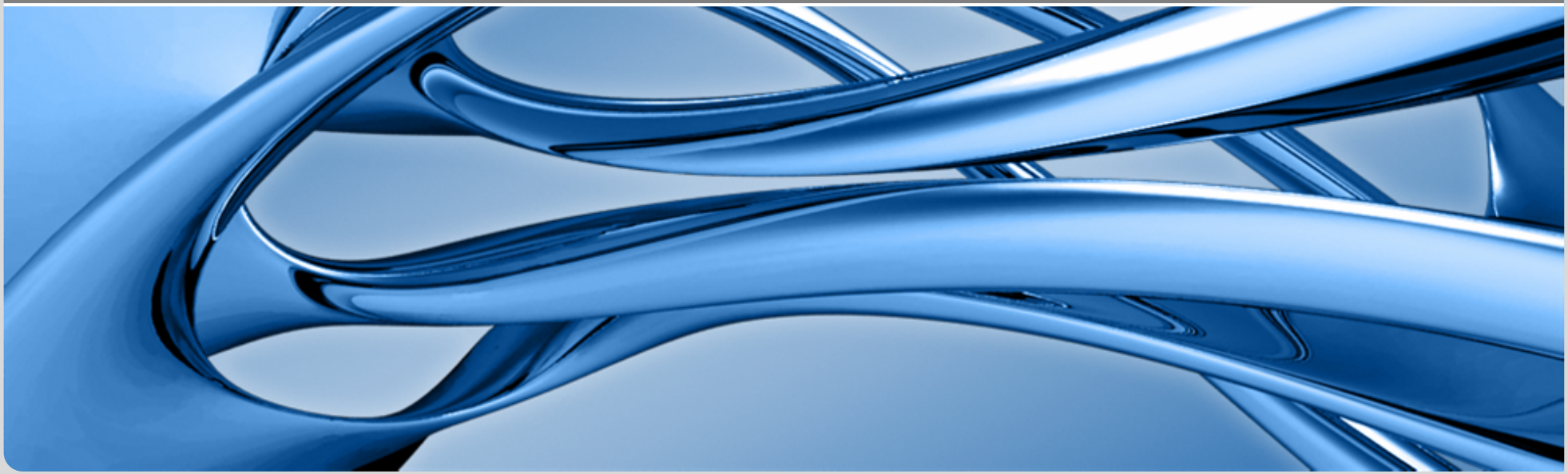

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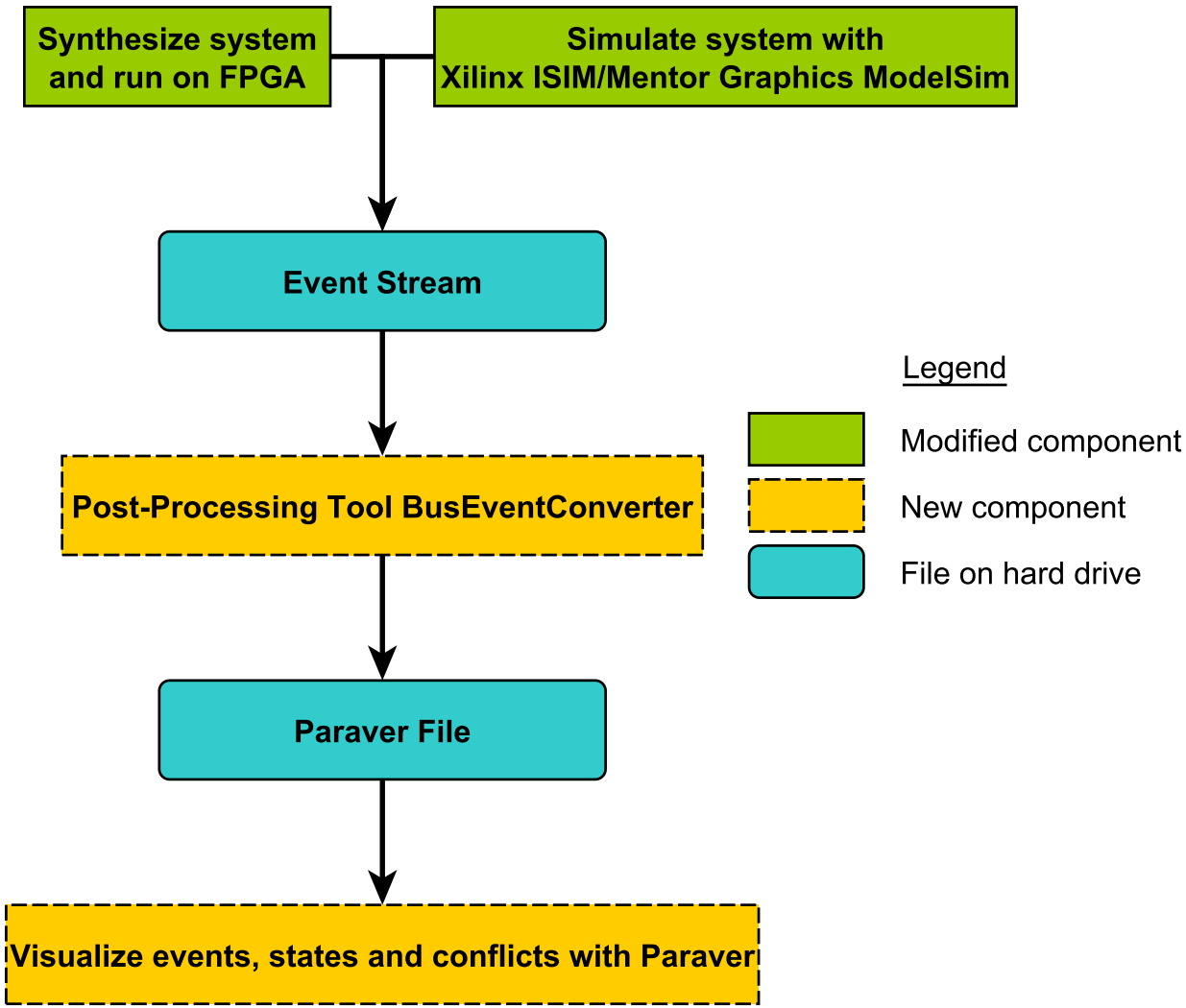
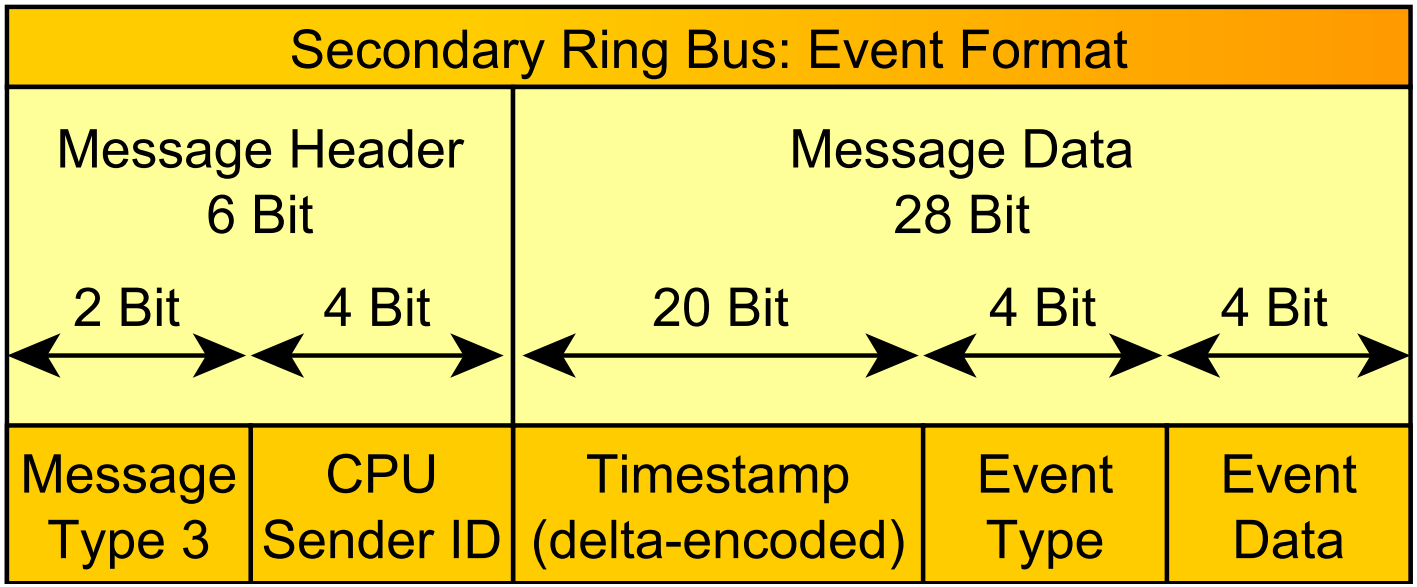
Additional slides

Workflow

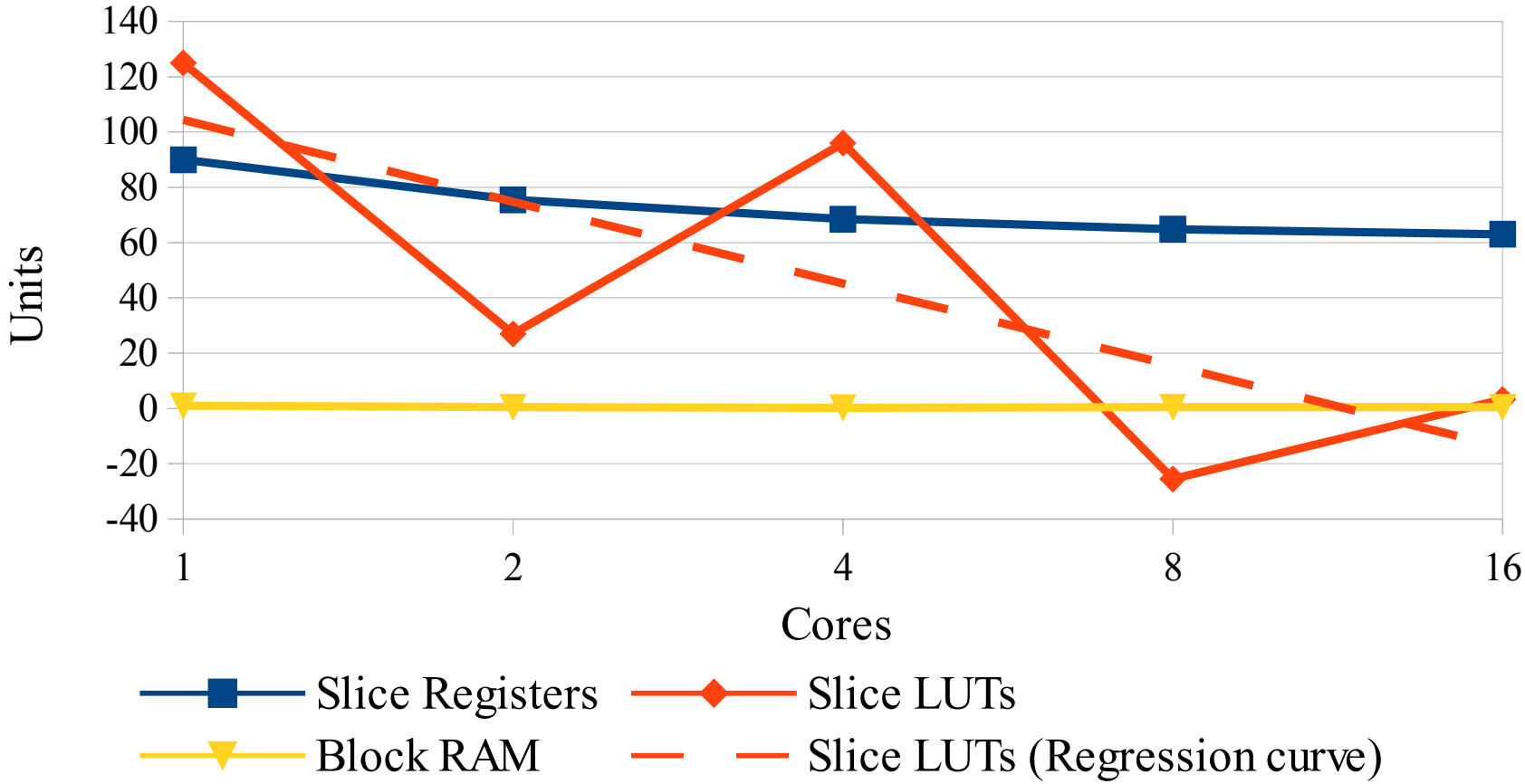

Synthesize system and run on FPGA
Simulate system with Xilinx ISIM/Mentor Graphics ModelSim
Event Stream
Post-Processing Tool BusEventConverter
Paraver File
Visualize events, states and conflicts with Paraver
Legend
Modified component
New component
File on hard drive

Event Diagram



Event diagram

FPGA Usage



TMbox FPGA Usage (with monitoring infrastructure) - Increase per Core